BYOC\_HW5:

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3.1) The listed below signals should be presented in the screen capture you need to attach to

your report. Show clock cycles 196-224 (following the end of the reset pulse, find i=196-224)

and make the values of all signals readable. For this you will probably need to show clocks

196-210 and 210-224 separately. These are the signals that can help you in “testing” the

DMem.

Note the some of these signals are inside the Host Intf :

1. CK

2. RESET

3. HOLD

4. i (the serial no. of the clock cycle)

5. PC\_reg

6. IR\_reg

7. MIPS\_DMem\_adrs

8. MIPS\_DMem\_wr\_data

9. MIPS\_DMem\_we

10. MIPS\_DMem\_rd\_data

11. DMem\_reg0

12. DMem\_reg1

13. DMem\_reg2

14. DMem\_reg3

15. DMem\_reg4

I=196-224 means CK cycles from 8440 ns to 9600 ns.

10

3.2) Explain in detail what happens, i.e., what do we see here. Note that it is essential to the

success of your future design that you will verify that the design does what we wanted it to

do in these CK cycles.

In that doc file you need also to answer the following questions:

3.3) What is the latency of an Rtype instruction? That is: How many nop-s should be inserted

between two consecutive Rtype instructions if the 2nd one uses the result of the 1st one?

3.4) Explain the limitation of beq that tests a register that is calculated by Rtype instruction.

As an example, translate the following C if statement:

for (i=0;i<10;i++) { … }

where i resides in register $3.

3.5) Are there any other limitations due to the pipeline structure in the instructions we

implemented (Rtype, addi, beq, bne, lw, sw, j)? How can we overcome these limitations

(e.g., by adding nop-s)? Try to list all of the **SW** & **HW** based solutions you can think of.